Electrical Characteristics (V^+=5 V_{DC}) (Note 3)

Parameter	Conditions	AS339N			Units
		Min	Typ	Max	
Input Offset Voltage	(Note 7)			±9	mV_{DC}
Input Offset Current	$I_{IN}(+) - I_{IN}(-)$, V_{CM}=0 V			±150	nA_{DC}
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with Output in Linear Range, V_{CM}=0 V (Note 4)			400	nA_{DC}
Input Common-Mode Voltage Range	V^+=+30 V_{DC} (Note 5)	0		V^+ -2	V_{DC}
Saturation Voltage	$V_{IN}(-)$=1 V_{DC}, $V_{IN}(+)$=0, I_{SINK}≤4 mA			700	mV_{DC}
Output Leakage Current	$V_{IN}(-)$=0, $V_{IN}(+)$=1 V_{DC}, V_O=30 V_{DC}			1.0	μA_{DC}

Note 1: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 2: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a valve greater than -0.3 V_{DC} (at 25°C).

Note 3: AS339N temperature specifications are limited to 0°C ≤ T_A ≤ +70°C.

Note 4: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 5: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V^+ -1.5 V at 25°C, but either or both inputs can go to 30 V_{DC} without damage, independent of the magnitude of V^+.

Note 6: The response time specified is a 100 mV input step with 5 mV overdrive.

Note 7: At output switch point, V_O≅1.4 V_{DC}, R_S=0 Ω with V^+ from 5 V_{DC} to 30 V_{DC}; and over the full input common-mode range (0 V_{DC} to V^+ -1.5 V_{DC}), at 25°C.

Low Power Low Offset Quad Comparator

General Description

The AS339N series consists of four independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max for all four comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The AS339N series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the AS339N series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

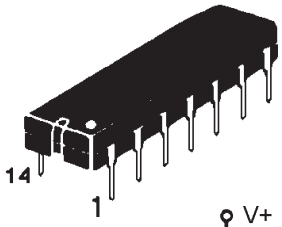
Advantages

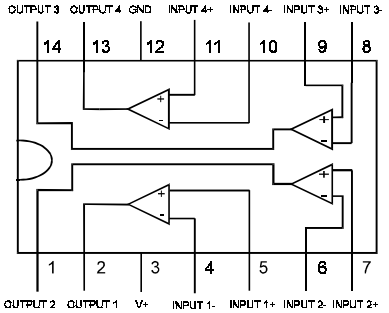
- High precision comparators.
- Reduced V_{OS} drift over temperature.
- Eliminates need for dual supplies.
- Allows sensing near ground.
- Compatible with all forms of logic.
- Power drain suitable for battery operation.

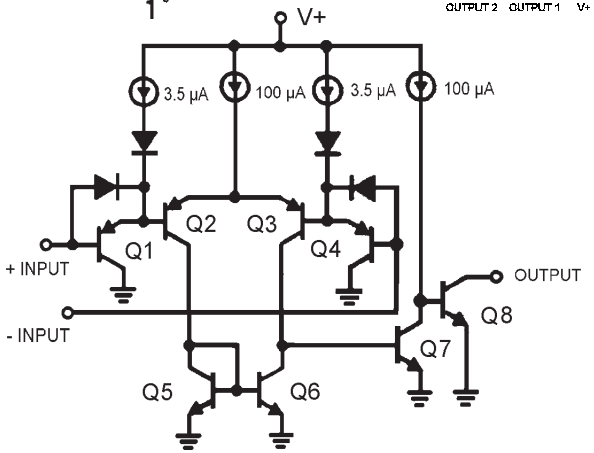
Features

- Wide single supply
  - Voltage range ..... 2.0 V_{DC} to 36 V_{DC}
  - or dual supplies ..... ± 1.0 V_{DC} to ± 18 V_{DC}
- Very low supply current drain (0.8 mA) – independent of supply voltage.
- Low input biasing current ..... 25 nA
- Low input offset current ..... ± 5 nA
  and offset voltage ..... ± 2 mV
- Input common-mode voltage range includes GND.
- Differential input voltage range equal to the power supply voltage.
- Low output saturation voltage ..... 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems.

Connection Diagram
Dual-in-Line Package







Schematic Diagram
(Each Comparator)

Absolute Maximum Ratings

Supply Voltage, V^+	36 V_{DC} or ±18 V_{DC}
Differential Input Voltage range (either input)	36 V_{DC}
Input Voltage	-0,3 V_{DC} to +36 V_{DC}
Input Current (V_{IN} <-0,3 V_{DC}) (Note 2)	50 mA
Power Dissipation Plastic DIP	500 mW
Output Short-Circuit to GND (Note 1)	Continuous
Operating Temperature Range	0^0C to 70^0C
Storage Temperature Range	-65^0C to $+150^0$C
Lead Temperature (Soldering, 10 seconds)	260^0C

Electrical Characteristics
T_{amb}=25°C, V^+ = +5,0 V_{DC}, unless otherwise stated

Parameter	Conditions	AS339N			Units
		Min	Typ	Max	
Input Offset Voltage	(Note 7)		±2.0	±5.0	mV_{DC}
Input Bias Current	I_{IN}(+) or I_{IN}(-) with Output in Linear Range, V_{CM}=0 V (Note 4)		25	250	nA_{DC}
Input Offset Current	I_{IN}(+) - I_{IN}(-), V_{CM}=0 V		±5	±50	nA_{DC}
Input Common-Mode Voltage Range	V^+=30 V_{DC} (Note 5)	0		V^+-1.5	V_{DC}
Supply Current	R_L= ∞ on all Comparators, R_L= ∞, V^+=36 V_{DC}		0.8 1	2.0 2.5	mA_{DC} mA_{DC}
Voltage Gain	V^+=15 V_{DC}, R_L>=15 kΩ V_0=1 V_{DC} to 11 V_{DC}	50	200		V/mV
Large Signal Response Time	V_{IN}=TTL Logic Swing, V_{REF}= =1.4 V_{DC}, V_{RL}=5 V_{DC}, R_L=5.1 kΩ		300		ns
Response Time	V_{RL}=5 V_{DC}, R_L=5.1 kΩ (Note 6)		1.3		µs
Output Sink Current	V_{IN}(-)=1V_{DC},V_{IN}(+)=0,V_O≤1.5V_{DC}	6.0	16		mA_{DC}
Saturation Voltage	V_{IN}(-)=1V_{DC}, V_{IN}(+)=0, I_{SINK}≤4mA		250	400	mV_{DC}
Output Leakage Current	V_{IN}(-)=0, V_{IN}(+)=1 V_{DC}, V_O=5 V_{DC}		0.1		nA_{DC}