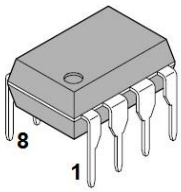
Ultraprecision Operational Amplifier with wide voltage range

FEATURES

- Ultralow offset voltage T_A = 25°C, 25 μV (typ)
- Wide range of supply voltages from ±3V to ±16,5V
- Outstanding offset voltage drift ± 0,1 μV/°C
- High long-term stability offset voltage
- Increased speed f_1 – 0,9 MHz, SR-0,36 V/μS
- Wide range of common mode input voltage ±13V
- Small input current 2nA (max)
- Excellent open-loop gain 10 V/μV typical
- Common-Mode Rejection Ratio 120dB

AS177



PDIP-8 (300 Mil, 2.54)

AS177D

SOIC-8 (150Mil, 1.27)

GENERAL DESCRIPTION

The AS177 op-amp has a very small offset voltage, which is achieved by trimming the microcircuit at the manufacturing stage and a wide range of supply voltages. The AS177 op-amp has low input currents and a high gain. Low offset voltage (U_{IO}) and high gain (A_U) make this op amp particularly attractive for use in instrumentation circuits.

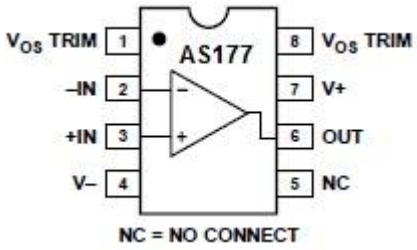
A wide input voltage range (U_{ICMAX}) in combination with a high common-mode input voltage attenuation coefficient (K_{CMR}) and high impedance provides high accuracy for non-inverting switching circuits. In deep feedback circuits, high values of linearity and accuracy can be achieved. The op-amp has high and normalized stability of the offset voltage and the difference of the input currents (I_{IO}) in time and from changes in ambient temperature.

The accuracy and stability of the AS177, even at high gain, combined with the freedom from external nulling have made the AS177 an industry standard for instrumentation applications.

PART NUMBER	PACKAGE	BODY SIZE (nom)
AS177	PDIP-8	300mil, 2.54 mm pitch
AS177D	SOIC-8	150mil, 1.27 mm pitch

Pin Information

(Top View)
PDIP-8
SOIC-8



Pin numbers Type of package	Symbol	Description
PDIP-8, SOIC-8		
1	**V_{OS} TRIM**	Balancing
2	**-IN**	Invert input
3	**+IN**	Noninvert input
4	**V^-(U_{CC2})**	Negative supply voltage
5	**NC**	No connect
6	**OUT**	Output
7	**V^+(U_{CC1})**	Positive supply voltage
8	**V_{OS} TRIM**	Balancing

Table 1 Maximum Ratings

Parametr, unit	Symbol	Maximum Permissible		Limit		Exposure time limit regime exploitation
		Min	Max	Min	Max	
Supply voltage, V	U_{CC1}	3	16,5	2	22	Two hours
	U_{CC2}	-16,5	-3	-22	-2	
Common-mode input voltages, V	U_{IC}	U_{CC2}+2V	U_{CC1}-2V	U_{CC2}	U_{CC1}	
Input differential voltage, V	U_{ID}	-	±5[1)]		±30[2)]	
Load resistance, kΩ	R_L	2		0,3		One minute with a duty cycle of 30 minutes..

Notes:
1) For $|U_{CC1,2}| \leq 6$ V, the input differential voltage is $|U_{CC1,2}|$-1 V.
2) In the range of operating temperatures up to 30° C, the absolute value of the voltages at any input should not exceed the value of the voltage of the power sources. At elevated temperatures, the maximum permissible U_{ID} decreases according to the dependence in Figure 3 or external current-limiting resistors at the inputs are used according to the dependence in Figure 4.

Table 2 Electrical parameters at U_{CC} = ± 3 V and U_{CC} = ± 15 V

Parameter, unit	Symbol	AS177, AS177D		Measuring mode	
		Min	Max	Ucc, V	R_L, kΩ
Output Voltage Swing, V	$U_{O\ max}$	1,8 10,5	-1,5 -10,5	±3 ±13,5	2
Input Offset Voltage1, μV	U_{IO}	-60 -40	60 40	±3 ±16,5	2
Input Bias Current, nA	I_I	-3 -3	3 3	±3 ±16,5	2
Input Offset Current, nA	I_{IO}	-2,5 -3,0	2,5 3,0	±3 ±16,5	2
Supply Current, mA	I_{CC}	- -	2,5 4,5	±3 ±16,5	2
Large Signal Voltage Gain	A_U	1500000	-	±3 ±13,5	2
Common Input Voltage, V	$U_{IC\ max}$	1,5 13	-1,5 -13	±3 ±15	2
Unity Gain Frequency, MHz	f_1	0,5	- -	±3 ±15	2
Common-Mode Rejection Ratio, dB	K_{CMR}	110	- -	±3 ±15	2
Power Supply Rejection Ratio, dB	K_{SVR}	100	- -	±3 ±15	2
Slew Rate, V/μS	SR	0,3	- -	±3 ±15	2
Average Input Offset Voltage Drift, μV/ºC	α_{UIO}	-0,8	0,8	±3 ±15	2
Average Input Offset Current Drift, pA/ºC	α_{IIO}	-30	30	±3 ±15	2

TYPICAL OPERATING CHARACTERISTICS

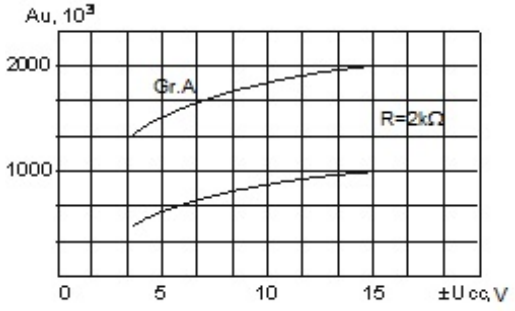


Fig. 1 Dependence of voltage gain on supply voltage

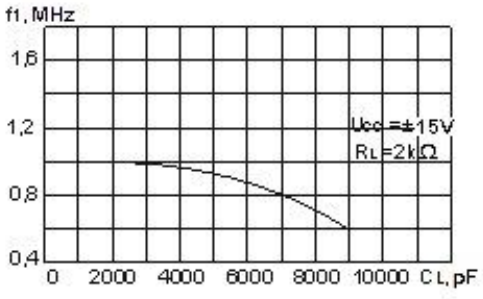


Fig. 2 The frequency dependence of a single gain from load capacity

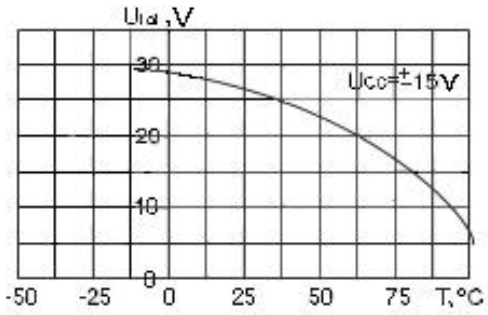


Fig. 3 Dependence of the limiting input differential voltage on the ambient temperature

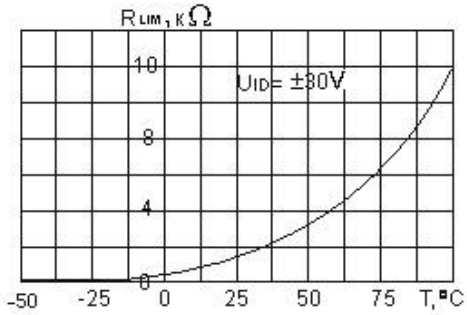


Fig. 4 Dependence of the minimum allowable input limiting resistance on the ambient temperature

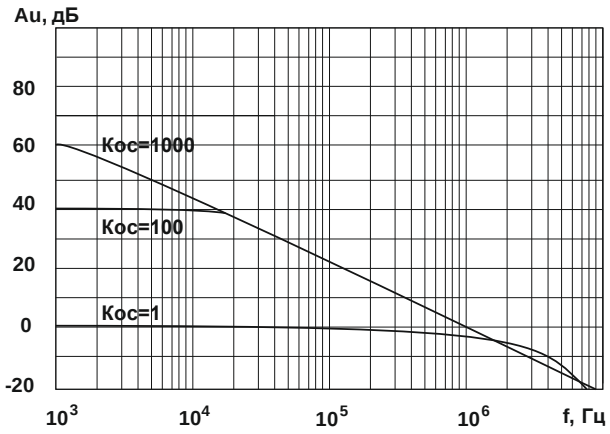


Fig. 5 The dependence of the amplitude-frequency characteristics for various gain with feedback

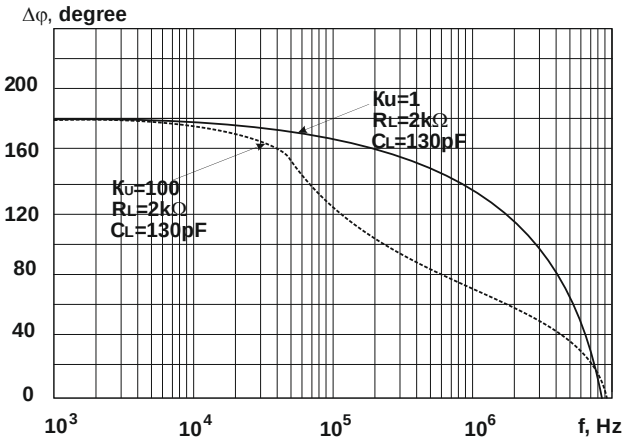


Fig. 6 Phase-frequency response for various feedback gain

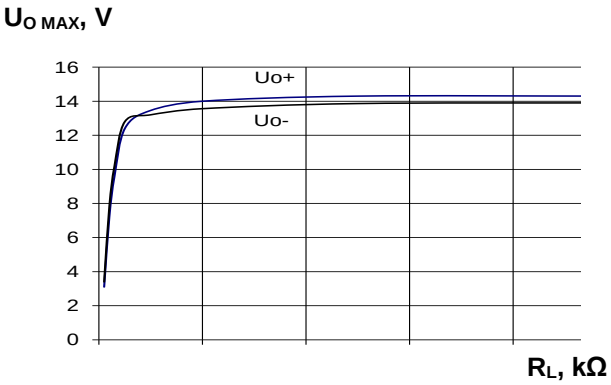


Fig. 7 The dependence of the maximum output voltage on the load resistance

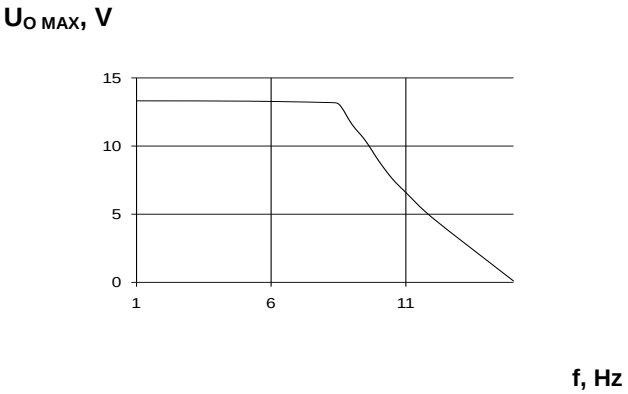


Fig. 8 The dependence of the maximum output voltage on the frequency

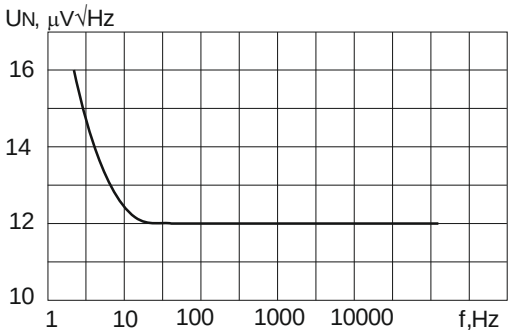


Fig. 9 Frequency dependence of the spectral density of noise voltage

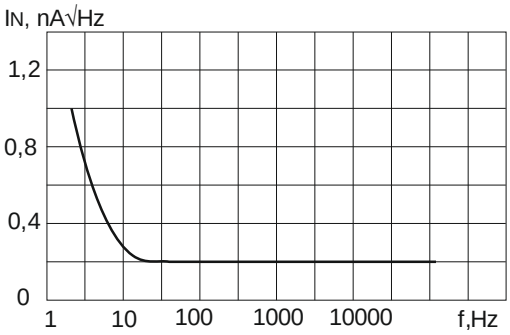


Fig. 10 The dependence of the spectral density of the noise current on the frequency

WIRING DIAGRAMS

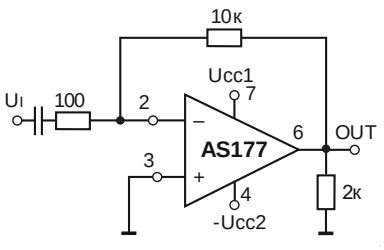


Fig. 11 Typical switching circuit

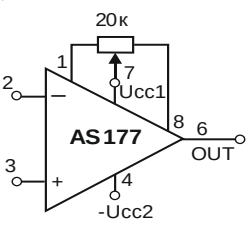


Fig. 12 Balancing scheme

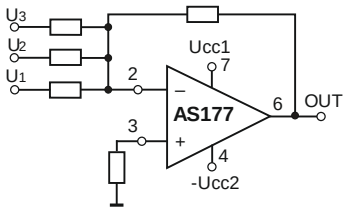


Fig. 13 Precision Summing Amplifier

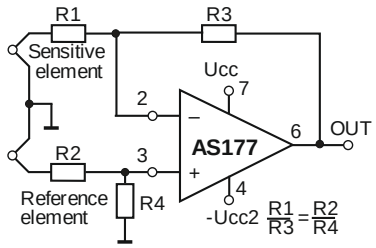
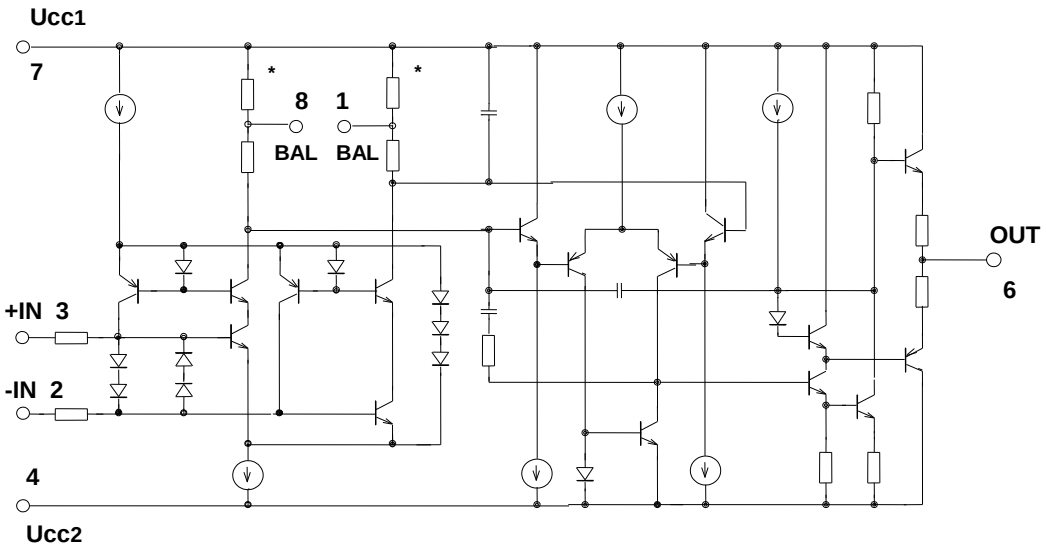


Fig. 14 Highly stable thermocouple amplifier

Figure 15. Simplified Schematic



OUTLINE DIMENSIONS
Dimensions show in inches and (millimeters)

AS177

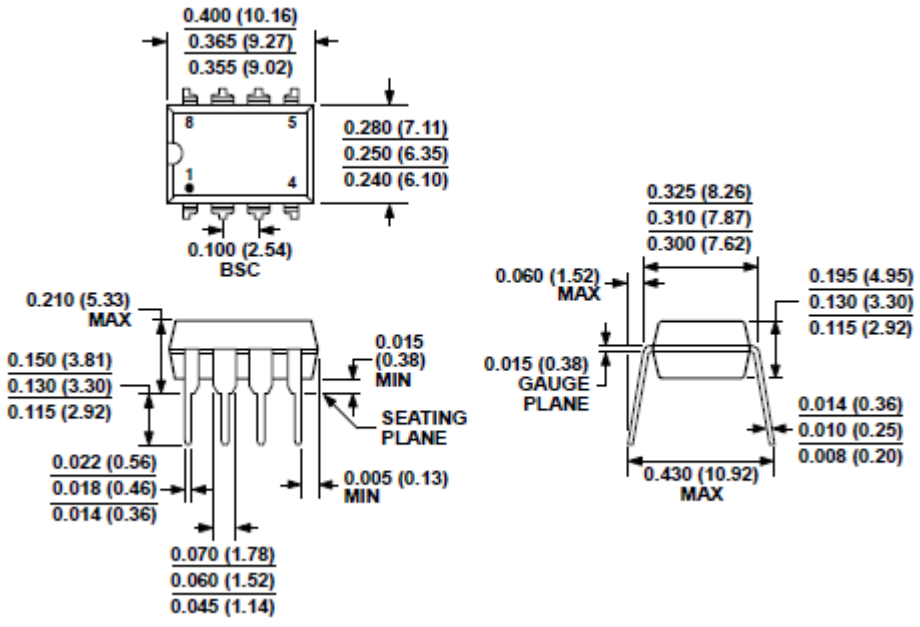


Figure 16. 8-Lead Plastic Dual In-Line Package (PDIP)

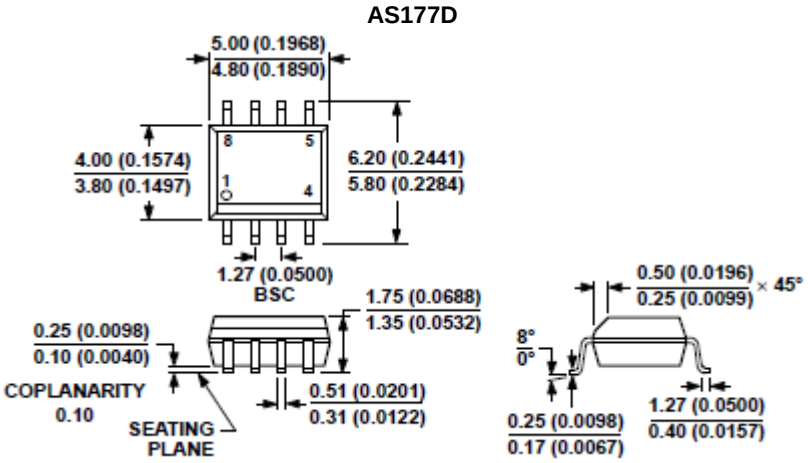


Figure 17. 8-Lead Standard Small Outline Package (SOIC_N)

Revision history

Date	Revision	Changes
09-Jan-2020	**1**	Initial version